

**REMARKS**

Applicant notes the filing of an Information Disclosure Statement herein on October 9, 2002, and notes that no copy of the PTO/SB/08 was returned with the outstanding Office Action.

Applicant respectfully requests that the information cited on the PTO/SB/08 be made of record herein.

The Office Action mailed October 24, 2002, has been received and reviewed. Claims 1 through 66 are currently pending in the application. Claims 9 and 21 through 58 have been withdrawn as being drawn to non-elected inventions. Claims 59 through 66 are allowed. Claims 1 through 8 and 10 through 20 stand rejected. Applicant has amended claims 1-5, 7, 8, 10, 19, and 20, has canceled claim 6, and respectfully requests reconsideration of the application as amended herein.

**Claim Objections**

Claims 3, 4 and 5 have been objected to because of writing informalities. Claims 3 through 5 have been amended herein, as suggested by the Examiner.

**Double Patenting Rejection Based on U.S. Patent No. 6,461,909**

Claims 1 through 8 and 10 through 20 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 6,461,909. In order to avoid further expenses and time delay, Applicant elects to expedite the prosecution of the present application by filing a terminal disclaimer to obviate the double patenting rejections in compliance with 37 CFR §1.321 (b) and (c). Applicant's filing of the terminal disclaimer should not be construed as acquiescence of the Examiner's double patenting or obviousness-type double patenting rejections. Attached is the terminal disclaimer and accompanying fee.

### 35 U.S.C. § 102(e) Anticipation Rejections

#### Anticipation Rejection Based on U.S. Patent No. 6,320,213 to Kirlin et al.

Claims 1, 2, 4, 15, and 19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kirlin et al. (U.S. Patent No. 6,320,213). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 has been amended to include the limitations recited in claim 6, i.e., that the diffusion barrier layer be formed through chemical vapor deposition of RuSi<sub>x</sub>O<sub>y</sub>. As acknowledged by the Examiner in the Office Action, Kirlin et al. does not anticipate claim 6 since it does not describe chemical vapor deposition of RuSi<sub>x</sub>O<sub>y</sub> over the surface of a semiconductor substrate assembly. Claims 2, 4, 15, and 19 all depend from and contain all of the limitations of amended claim 1. In view of the amendment to claim 1, applicant believes that claims 1, 2, 4, 15, and 19 are now in condition for allowance and respectfully requests withdrawal of the rejections.

### ENTRY OF AMENDMENTS

The amendments to claims 1-5, 7, 8, 10, 19, and 20 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Dependent claim 10 has been amended to include all of the limitations of claim 1 and, thus, to make claim 10 an independent claim. Further, the amendments do not raise new issues or require a further search.

**CONCLUSION**

Claims 1-5, 7, 8, 10-20 (and previously allowed claims 59-66) are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



Edgar R. Cataxinos  
Registration No. 39,931  
Attorney for Applicant(s)  
**TRASKBRITT**  
P.O. Box 2550  
Salt Lake City, Utah 84110-2550  
Telephone: 801-532-1922

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method for forming a semiconductor device structure comprising:  
providing a semiconductor substrate assembly having a surface; and  
depositing RuSi<sub>x</sub>O<sub>y</sub> by chemical vapor deposition to form [forming] a diffusion barrier layer over  
at least a portion of the surface[, wherein the diffusion barrier layer comprises RuSi<sub>x</sub>O<sub>y</sub>].
  2. (Twice amended) The method of claim 1, wherein depositing RuSi<sub>x</sub>O<sub>y</sub> by  
chemical vapor deposition [forming the diffusion barrier layer over at least a portion of the  
surface further] comprises [forming a] depositing the layer of RuSi<sub>x</sub>O<sub>y</sub> where x is in a range of  
about 0.01 to about 10.
  3. (Twice amended) The method of claim 2, wherein depositing RuSi<sub>x</sub>O<sub>y</sub> by chemical  
vapor deposition [forming the diffusion barrier layer over at least a portion of the surface further]  
comprises [forming a] depositing the layer of RuSi<sub>x</sub>O<sub>y</sub> where x is about 0.4.
  4. (Twice amended) The method of claim 1, wherein depositing RuSi<sub>x</sub>O<sub>y</sub> by chemical  
vapor deposition [forming the diffusion barrier layer over at least a portion of the surface further]  
comprises [forming a] depositing the layer of RuSi<sub>x</sub>O<sub>y</sub> where y is in a range of about 0.01 to  
about 10.
  5. (Twice amended) The method of claim 4, wherein forming the diffusion barrier layer  
over at least a portion of the surface [further] comprises forming [a] the layer of RuSi<sub>x</sub>O<sub>y</sub> where y  
is about 0.05.
- Cancel claim 6.
7. (Twice amended) The method of claim 1, wherein depositing the RuSi<sub>x</sub>O<sub>y</sub> [forming  
the diffusion barrier layer includes] comprises depositing RuSi<sub>x</sub>O<sub>y</sub> by atomic layer deposition.

8. (Twice amended) The method of claim 7, wherein depositing the RuSi<sub>x</sub>O<sub>y</sub> [forming the diffusion barrier layer includes] comprises depositing three to five monolayers of RuSi<sub>x</sub>O<sub>y</sub>.

10. (Amended) [The method of claim 1, wherein forming said diffusion barrier layer comprises:] A method for forming a semiconductor device structure comprising:  
providing a semiconductor substrate assembly having a surface;  
forming a layer of ruthenium relative to a silicon-containing region; and  
performing an anneal in an oxidizing atmosphere to form RuSi<sub>x</sub>O<sub>y</sub> from the layer of ruthenium and the silicon-containing region.

19. (Amended) The method of claim 1, wherein [forming said diffusion barrier layer comprises forming a diffusion barrier layer] said RuSi<sub>x</sub>O<sub>y</sub> is deposited in an oxidizing atmosphere.

20. (Twice amended) The method of claim 19, wherein [forming the diffusion barrier layer in an oxidizing atmosphere comprises forming a diffusion barrier layer] said RuSi<sub>x</sub>O<sub>y</sub> is deposited in an atmosphere including an oxidizing gas.